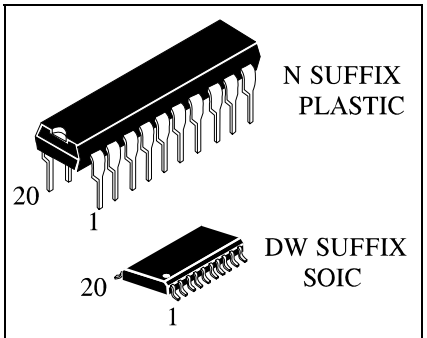
IN74LS245

Octal 3-State Noninverting Bus Transceiver

These octal bus transceiver are designed for asynchronous two-way communication between data buses. The control function implementation minimized external timing requirements.

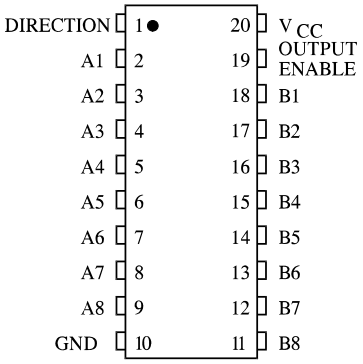
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the directional control (DIR) input. The enable input(E) can be used to disable the device so that the buses are effectively isolated.

- Bidirectional Bus Transceiver in a High-Density 20-Pin Package
- 3-state Outputs Dirve Bus Lines Directly
- P-N-P Inputs D-C Loading on Bus Lines
- Hysteresis at Bus Inputs Improve Noise Margins
- Typical Propagation Delay Times; Port to Port … 8 ns

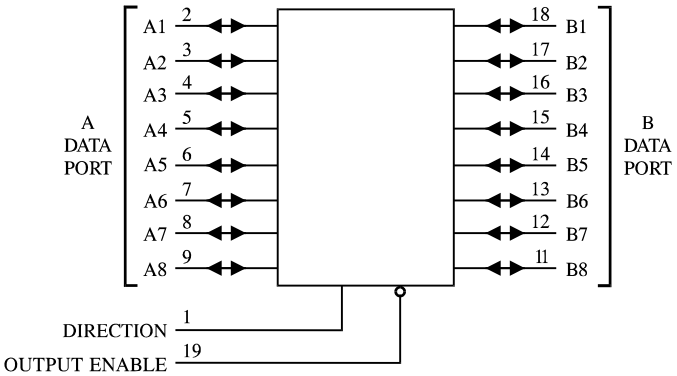


ORDERING INFORMATION
IN74LS245N Plastic
IN74LS245DW SOIC
T_A = 0° to 70° C
for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High Impedance State)

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
I_{OH}	High Level Output Current		-15	mA
I_{OL}	Low Level Output Current		24	mA
T_A	Ambient Temperature Range	0	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter		Test Conditions	Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage		V_{CC} = min, I_{IN} = -18 mA		-1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = min, I_{OH} = -1.0 mA	2.7		V
			V_{CC} = min, I_{OH} = -3.0 mA	2.4		
			V_{CC} = min, I_{OH} = -15 mA	2.0		
V_{OL}	Low Level Output Voltage		V_{CC} = min, I_{OL} = 12 mA		0.4	V
			V_{CC} = min, I_{OL} = 24 mA		0.5	
$V_{T+} - V_{T-}$	Hysteresis		V_{CC} = min	0.2		V
I_{OZH}	Output Off Current HIGH		V_{CC} = max, V_{OUT} = 2.7 V		20	µA
I_{OZL}	Output Off Current LOW		V_{CC} = max, V_{OUT} = 0.4 V		-0.2	mA
I_{IH}	High Level Input Current		V_{CC} = max, V_{IN} = 2.7 V		20	µA
			V_{CC} = max, V_{IN} = 5.5 V (A or B)		0.1	mA
			V_{CC} = max, V_{IN} = 7.0 V for Pin1, Pin 19		0.1	
I_{IL}	Low Level Input Current		V_{CC} = max, V_{IN} = 0.4 V		-0.2	mA
I_O	Output Short Circuit Current		V_{CC} = max, V_O =0 V (Note 1)	-40	-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = max		70	mA
		Outputs Low	Outputs open		90	
		All outputs disable			95	

Note 1: Not more thanone output should be shorted at a time, and duration of the short-circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, t_r = 15 ns,, t_f = 6.0 ns)

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (from A or B to Output)	C_L = 45 pF, R_L = 667 Ω		12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (from A or B to Output)			12	ns
t_{PZH}	Output Enable Time to High Level (from OE to Output)			40	ns
t_{PZL}	Output Enable Time to Low Level (from OE to Output)			40	ns
t_{PHZ}	Output Disable Time from High Level (from OE to Output)	C_L = 5 pF, R_L = 667 Ω		25	ns
t_{PLZ}	Output Disable Time from Low Level (from OE to Output)			25	ns

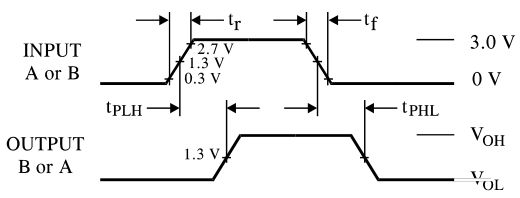
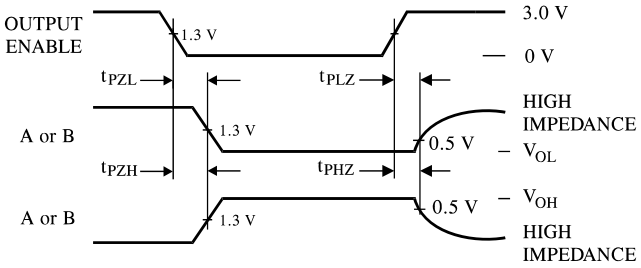
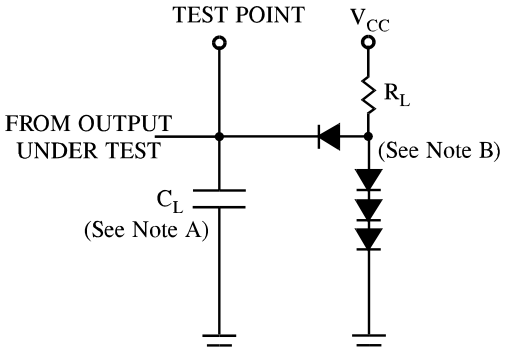


Figure 1. Switching Waveforms
(See Figure 3)



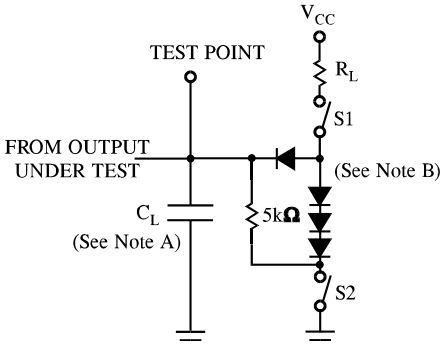
t_{PZL} - S1 closed, S2 opened
t_{PZH}- S1 opened, S2 closed
t_{PLZ}, t_{PHZ} - S1 and S2 closed

Figure 2. Switching Waveforms
(See Figure 4)



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 3. Test Circuit



NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM