IN74HCT163A

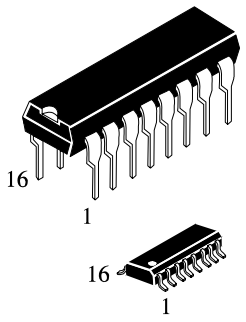
Presettable Counters
High-Performance Silicon-Gate CMOS

The IN74HCT163A is identical in pinout to the LS/ALS163. The IN74HCT163 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The IN74HCT163A is programmable 4-bit synchronous counter that feature parallel Load, synchronous Reset, a Carry Output for cascading and count-enable controls.

The IN74HCT163A is binary counter with synchronous Reset.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA

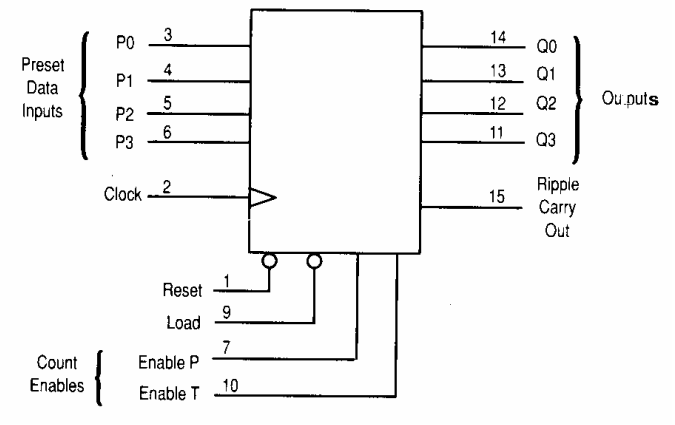


N SUFFIX
PLASTIC

D SUFFIX
SOIC

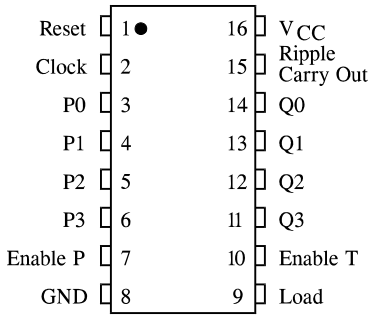
ORDERING INFORMATION
IN74HCT163AN Plastic
IN74HCT163AD SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs				Function
Reset	Load	Enable P	Enable T	Clock	Q0	Q1	Q2	Q3	
L	X	X	X	⌐	L	L	L	L	Reset to "0"
H	L	X	X	⌐	P0	P1	P2	P3	Preset Data
H	H	X	L	⌐	No change				No count
H	H	L	X	⌐	No change				No count
H	H	H	H	⌐	Count up				Count
X	X	X	X	¬	No change				No count

X=don't care
P0,P1,P2,P3 = logic level of Data inputs
Ripple Carry Out = Enable T • Q0 • Q1 • Q2 • Q3

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \leq 20$ μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \leq 20$ μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	5.5	4.0	40	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{IN} = 2.4 V, Any One Input V_{IN}=V_{CC} or GND, Other Inputs		≥-55°C		25°C to 125°C	mA
		I_{OUT}=0μA	5.5	2.9		2.4	

AC ELECTRICAL CHARACTERISTICS(V_{CC}=5.0 V ± 10%, C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (Figures 1,6)	30	24	20	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	34	43	51	ns
t_{PHL}	(Figures 1,6)	41	51	62	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 2,6)	32	40	48	ns
t_{PHL}		39	49	59	ns
t_{PLH}	Maximum Propagation Delay, Clock to Ripple	35	44	53	ns
t_{PHL}	Carry Out (Figures 1,6)	43	54	65	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output, (Figures 1 and 6)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Gate)	Typical @25°C,V_{CC}=5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}+\Delta I_{CC}V_{CC}$	60	

TIMING REQUIREMENTS (V_{CC}=5.0 V ± 10%, C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 4)	30	38	45	ns
t_{su}	Minimum Setup Time, Load to Clock (Figure 4)	27	34	41	ns
t_{su}	Minimum Setup Time, Reset to Clock (Figure 3)	32	40	48	ns
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 5)	40	50	60	ns
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 4)	10	13	15	ns
t_h	Minimum Hold Time, Clock to Load (Figure 4)	3	3	3	ns
t_h	Minimum Hold Time, Clock to Reset (Figure 3)	3	3	3	ns
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 5)	3	3	3	ns
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 4)	25	31	38	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	16	20	24	ns
t_w	Minimum Pulse Width, Reset (Figure 4)	16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	500	500	500	ns

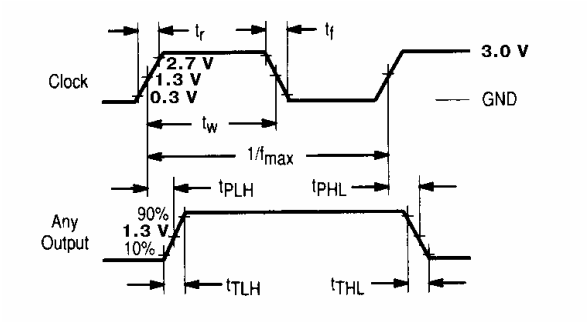


Figure 1. Switching Waveforms

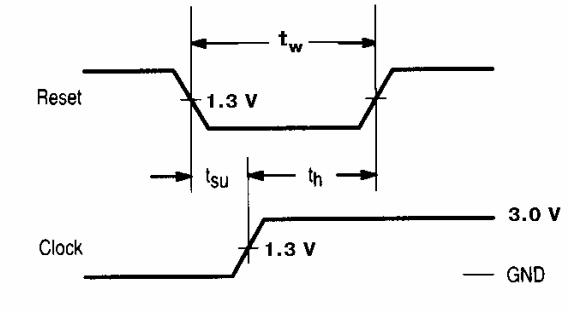


Figure 2. Switching Waveforms

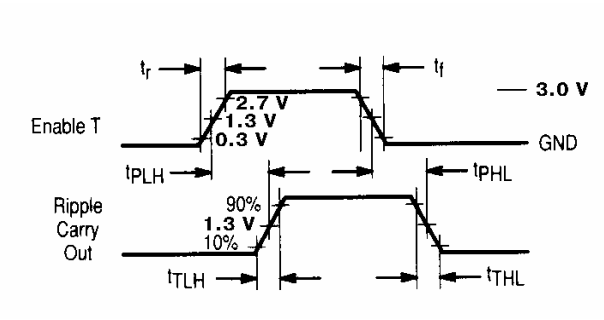


Figure 3. Switching Waveforms

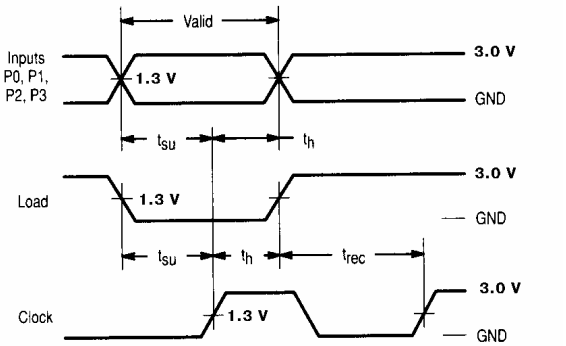


Figure 4. Switching Waveforms

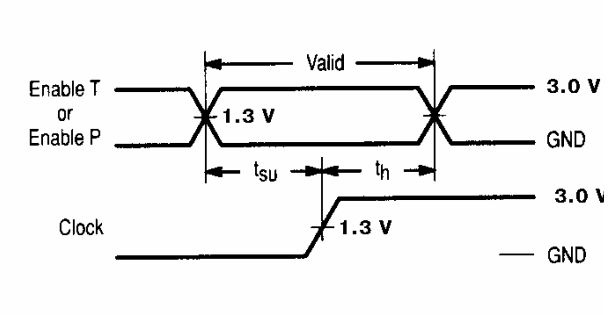


Figure 5. Switching Waveforms

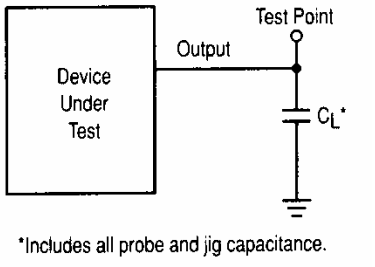
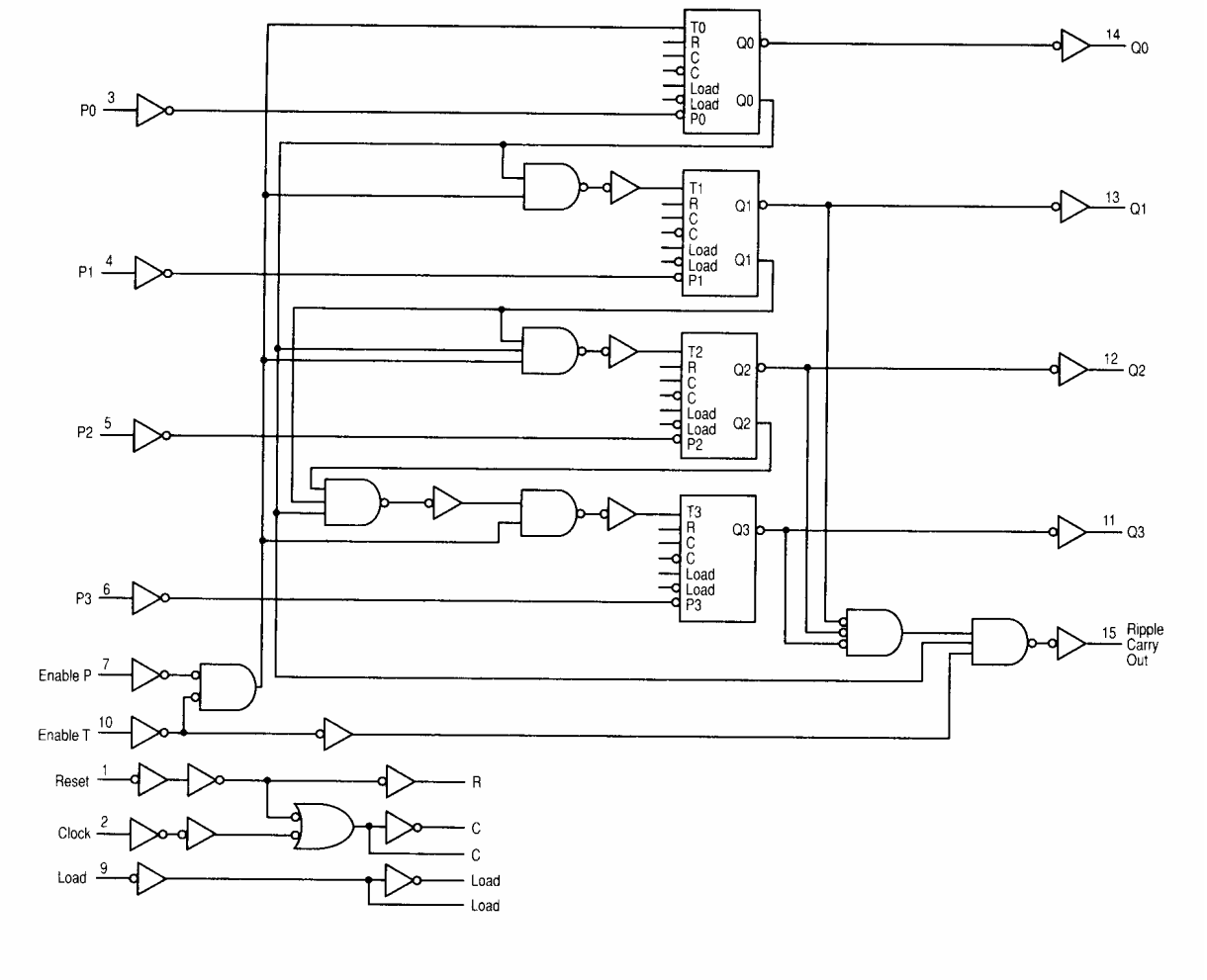


Figure 6. Test Circuit

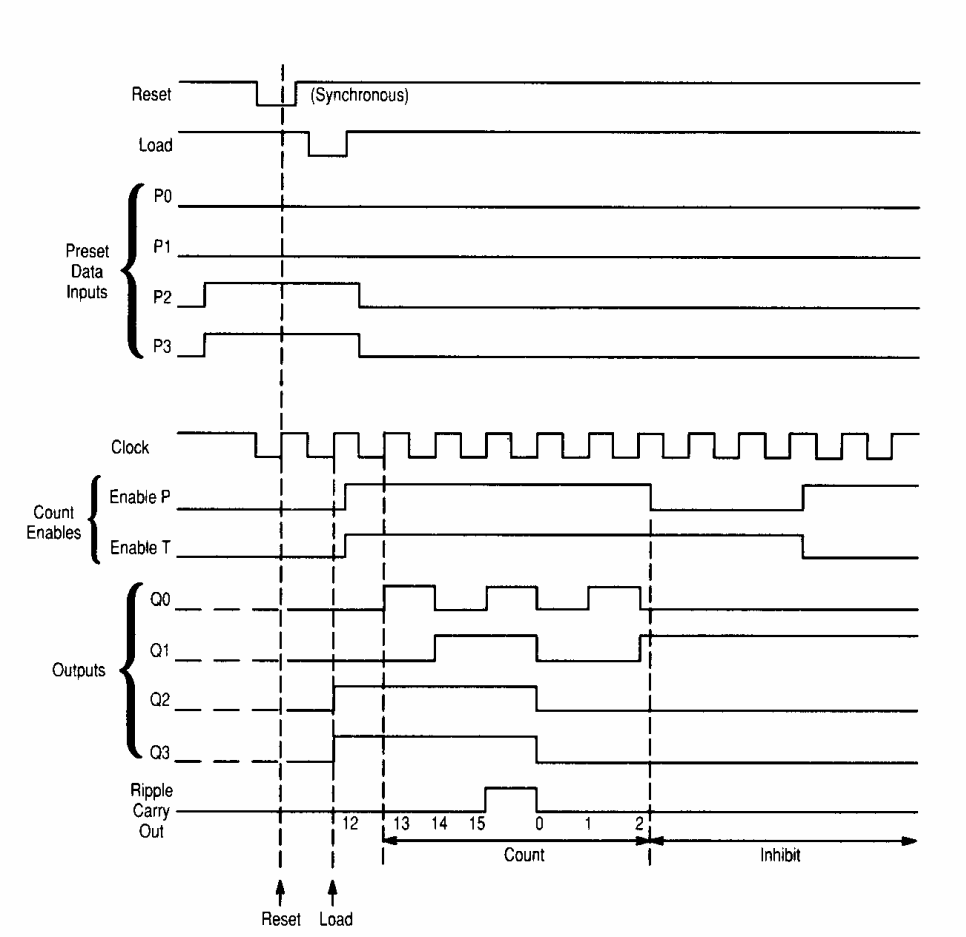


V_{CC} = Pin 16
GND = Pin 8

The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

Figure 7.Expanded logic diagram

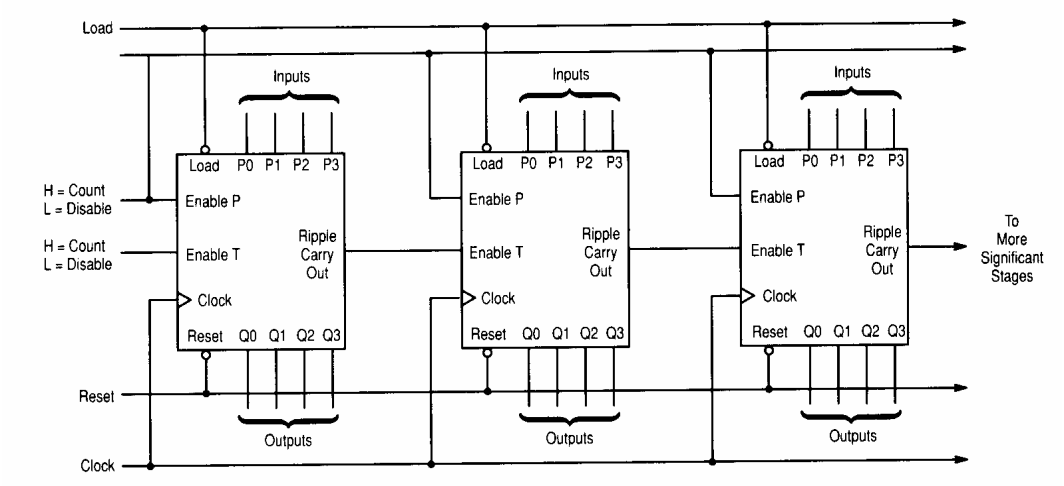


Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

Figure 8. Timing Diagram

TYPICAL APPLICATIONS CASCADING



Note: When used in these cascaded configurations the clock f_{max} guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and clock.

Figure 9. N-Bit Synchronous Counters

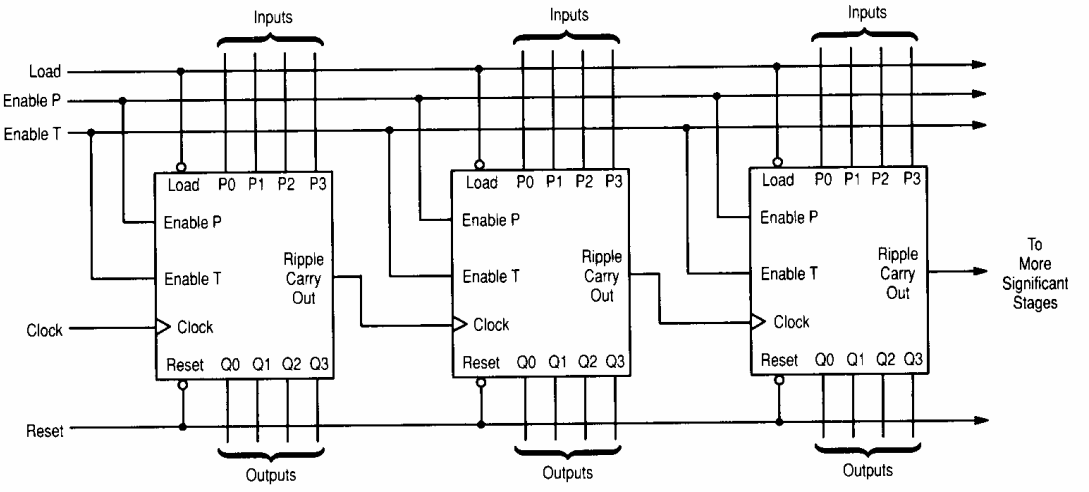


Figure 10. Nibble Ripple Counter